Serial No. 09/893,598
Docket No. 01USFP644-M.K.

REMARKS

Claims 1-20 are presently pending in this application. Applicant gratefully acknowledges the Examiner for taking time from his busy schedule to conduct a personal interview with Applicant's representative on April 28, 2004. The claim amendments above result from discussion during that personal interview.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

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To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Attorney's Deposit Account No. 50-0481 and please credit any excess fees to such deposit account.

Respectfully Submitted,

Date: 5/12/04

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CERTIFICATION OF TRANSMISSION

I certify that I transmitted via facsimile to (703) 872-9306 this Supplemental Amendment under 37 CFR §1.111 to Examiner P. Bell on May 12, 2004.

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EXEMPLARY CORRELATION BETWEEN CLAIM LANGUAGE AND FIGURES

1. (Currently amended) A semiconductor circuit system comprising:

a first signal line **(e.g., 5)**; and

n circuit sections **(e.g., 2-1,... 2-n)**, where n is an integer equal to or more than 2, each of which includes an input terminal and an output terminal,

wherein said input terminals of only predetermined k ones **(e.g., k = 2, in Figure 4)** of said n circuit sections are connected to said first signal line **(e.g., 5)**, where k is an integer satisfying $2 < k < n$, and

said output terminal of an m^{th} one of said n circuit sections is connected to said input terminal of an $(m+k)^{th}$ one of said n circuit sections, where $1 < m < n-k$. **(e.g., note k = 2 in Figure 4, therefore, output 4-1 of section 2-1 becomes input 3-3 in section 2-3. In conventional configurations, output 4-1 would become input 3-2 in section 2-2.)**

2. (Original) The semiconductor circuit system according to claim 1, wherein each of said n circuit sections starts an operation in response to a start signal **(e.g., 7)** on said first signal line and stops the operation a predetermined time after the start of the operation.

3. (Currently amended) The semiconductor circuit system according to claim 1, wherein each of said n circuit sections ~~includes~~ comprises:

a differential input circuit; and

a register circuit, ~~and~~

wherein said differential input circuit is activated in response to a start signal **(e.g., 7)** on said first signal line to start an operation and stops the operation a predetermined time after the start of the operation.

4. (Previously presented) The semiconductor circuit system according to claim 1, wherein each of said n circuit sections comprises:

a differential input circuit **(e.g., 13)**; and

a register circuit **(e.g., 15)**,

wherein said differential input circuit is activated in response to a start signal **(7)**on said first signal line to start an operation and stops the operation in response to an output from said register circuit.

5. (Original) The semiconductor circuit system according to claim 4, wherein the output **(e.g., D4)** from said register circuit **(e.g., 15)** is used as said start signal for a next one of said n circuit sections which is connected to said circuit section.

6. (Currently amended) The semiconductor circuit system according to claim 1, wherein each of said n circuit sections **(e.g., section 2-I in figure 4)** comprises:

a plurality of differential input circuits **(e.g., 13,14,18 of fig. 6**;

a plurality **(e.g., 15,16)**of register circuits connected to output terminals of said plurality of differential input circuits, respectively; and

a control circuit **(e.g., 11,12, 19)** including a latch circuit **(e.g., 19)**, said control circuit connected with at least one **(e.g., 15)** of said plurality of register circuits as a specific register circuit **(e.g., 15)** and said plurality of differential input circuits,

wherein said specific register circuit **(e.g., 15)** executes a predetermined operation using a first signal **(e.g., D6; note: along with SPIN 7)** outputted from a corresponding one **(e.g., 13)** of said plurality of differential input circuits, and outputs a second signal **(e.g., D4)** to said latch circuit **(e.g., 19)** when the operation ends, and

said control circuit activates said plurality of differential input circuits in response to a third signal **(e.g., D1)** to operate and stops the operations of said plurality of differential input circuits in response to said second signal.

7. (Previously presented) The semiconductor circuit system according to claim 6, wherein:

said plurality of register circuits comprises at least one set **(e.g., 15)** of registers and at least one set **(e.g., 16,18)** of data registers, and

said specific register circuit includes said set **(e.g., 15)** of registers.

8. (Original) The semiconductor circuit system according to claim 7, wherein each of said registers **(e.g., 15)** outputs a pulse signal to a corresponding one of said data registers **(e.g., 16)** when said first signal **(e.g., D6, SPIN)** is supplied, such that data are written in a corresponding one of said data registers **(e.g., 16)**, and propagates said first signal to a next one of said registers **(e.g., 15)** which is connected to said register, and

a last one of said registers **(e.g., 15-j)** outputs said first signal **(e.g., D6, SPIN)** as said second signal **(e.g., D4)**.

9. (Original) The semiconductor circuit system according to claim 6, wherein said control circuit comprises:

a first latch **(e.g., 19)** which latches said second signal;

a second latch **(e.g., 11)** which is set in response to said third signal **(e.g., D1)** and is reset in response to said second signal **(e.g., D4)** latched by said first latch **(e.g., 19)**; and

a switch **(e.g., 12)** which activates said plurality of differential input circuits when said second latch is set and inactivates said plurality of differential input circuits when said second latch is reset.

10. (Currently amended) The semiconductor circuit system according to claim 1, wherein said n circuit sections are respectively provided ~~for~~ on different semiconductor chips~~, respectively~~.

11. **(see claim 6)** (Currently amended) A semiconductor circuit comprising:

a plurality of differential input circuits;

a plurality of register circuits connected to output terminals of said plurality of differential input circuits, respectively; and

a control circuit including a latch circuit, said control circuit connected with at least one of said plurality of register circuits as a specific register circuit and said plurality of differential input circuits,

wherein said specific register circuit executes a predetermined operation using a first signal outputted from a corresponding one of said plurality of differential input circuits, and outputs a second signal to said latch circuit when the operation ends, and

said control circuit activates said plurality of differential input circuits in response to a third signal to operate and stops the operations of said plurality of differential input circuits in response to said second signal.

12. **(see claim 7)** (Original) The semiconductor circuit according to claim 11, wherein said plurality of register circuits comprises at least one set of registers and at least one set of data registers, and

said specific register circuit includes said set of registers.

13. **(see claim 8)** (Original) The semiconductor circuit according to claim 12, wherein each of said registers outputs a pulse signal to a corresponding one of said data registers when said first signal is supplied, such that data are written in a corresponding one of said data registers, and propagates said first signal to a next one of said registers which is connected to said register, and

a last one of said registers outputs said first signal as said second signal.

14. **(see claim 9)** (Original) The semiconductor circuit according to claim 11, wherein said control circuit comprises:

a first latch which latches said second signal;

a second latch which is set in response to said third signal and is reset in response to said second signal latched by said first latch; and

a switch which activates said plurality of differential input circuits when said second latch is set and inactivates said plurality of differential input circuits when said second latch is reset.

15. (Currently amended) A liquid crystal display apparatus, comprising:

a liquid crystal display panel; **(e.g., 101)**

a horizontal drive unit **(e.g., 104)**; and

a vertical drive unit **(e.g., 103)**,

wherein said horizontal drive unit further comprises: **(see claim 1)**

a first signal line; and

n circuit sections, where n is an integer equal to or greater than 2, each of which said n circuit sections has an input terminal and an output terminal, input terminals of only predetermined k ones of said n circuit sections are connected to said first signal line, where k is an integer satisfying $2 \leq k < n$, and said output terminal of an m^{th} one of said n circuit sections is connected to said input terminal of an $(m+k)^{th}$ one of said n circuit sections, where $1 \leq m \leq n-k$.

16. **(see claim 2)** (Previously presented) The apparatus according to claim 15, wherein each of said n circuit sections starts an operation in response to a start signal on said first signal line and stops the operation a predetermined time after the start of the operation.

17. **(see claim 3)** (Previously presented) The apparatus according to claim 15, wherein each of said n circuit sections includes a differential input circuit and a register circuit, and

said differential input circuit is activated in response to a start signal on said first signal line to start an operation and stops the operation a predetermined time after the start of the operation.

18. **(see claim 6)** (Currently amended) The apparatus according to claim 15, wherein each of said n circuit sections comprises:

a plurality of differential input circuits;

a plurality of register circuits connected to output terminals of said plurality of differential input circuits, respectively; and

a control circuit including a latch circuit, said control circuit connected with at least one of said plurality of register circuits as a specific register circuit and said plurality of differential input circuits,

wherein said specific register circuit executes a predetermined operation using a first signal outputted from a corresponding one of said plurality of differential input circuits, and outputs a second signal to said latch circuit when the operation ends, and

said control circuit activates said plurality of differential input circuits in response to a third signal to operate and stops the operations of said plurality of differential input circuits in response to said second signal.

19. **(see claim 9)** (Previously presented) The apparatus according to claim 18, wherein said control circuit comprises:

a first latch which latches said second signal;

a second latch which is set in response to said third signal and is reset in response to said second signal latched by said first latch; and

a switch which activates said plurality of differential input circuits when said second

latch is set and inactivates said plurality of differential input circuits when said second latch is reset.

20. **(see claim 1)** (Currently amended) A method of reducing power consumption in a liquid crystal display device having a liquid crystal display panel with a horizontal drive unit and a vertical drive unit, wherein said horizontal drive unit comprises a first signal line and n circuit sections, where n is an integer equal to or greater than 2, each of which said n circuit sections has an input terminal and an output terminal, said method comprising:

connecting said first signal line to input terminals of only predetermined k ones of said n circuit sections, where k is an integer satisfying $2 \leq k < n$; and

connecting said output terminal of an m^{th} one of said n circuit sections to said input terminal of an $(m+k)^{th}$ one of said n circuit sections, where $1 \leq m \leq n-k$.